

Samsung
NP-N100S, NP-N102S

Eric-VE-R

ENE micom

CPU : INTEL CEDARVIEW-M
Chip Set : INTEL TIGERPOINT-M
Remarks : DC, DDR3

Model Name : Eric-VE-R
PCB Part No : BA41-01868A(GCE)
BA41-01869A(GBM)
BA41-01871A(PIOTEC)

Dev. Step : PR
Revision : 1.0
T.R. Date : 2011.12.12

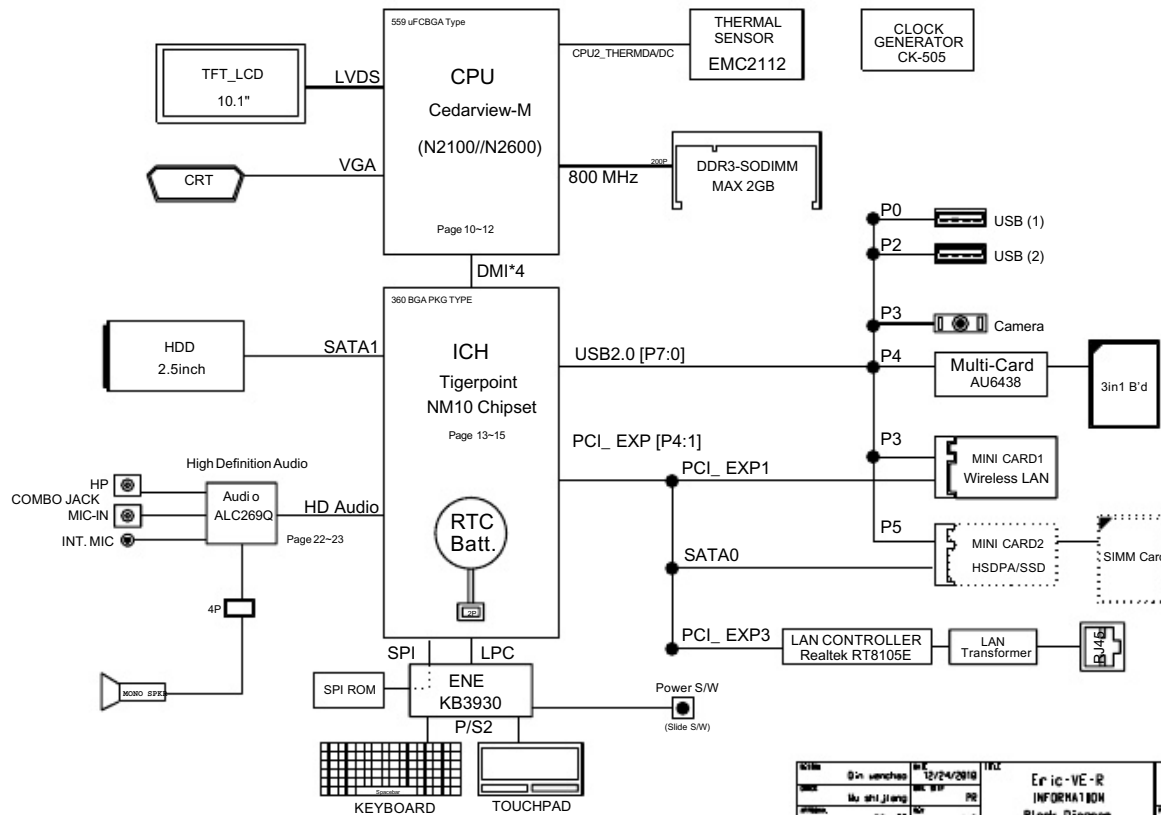
DRAW	CHECK	APPROVAL
Qin Wenchao	Wu shijiang	BC LEE

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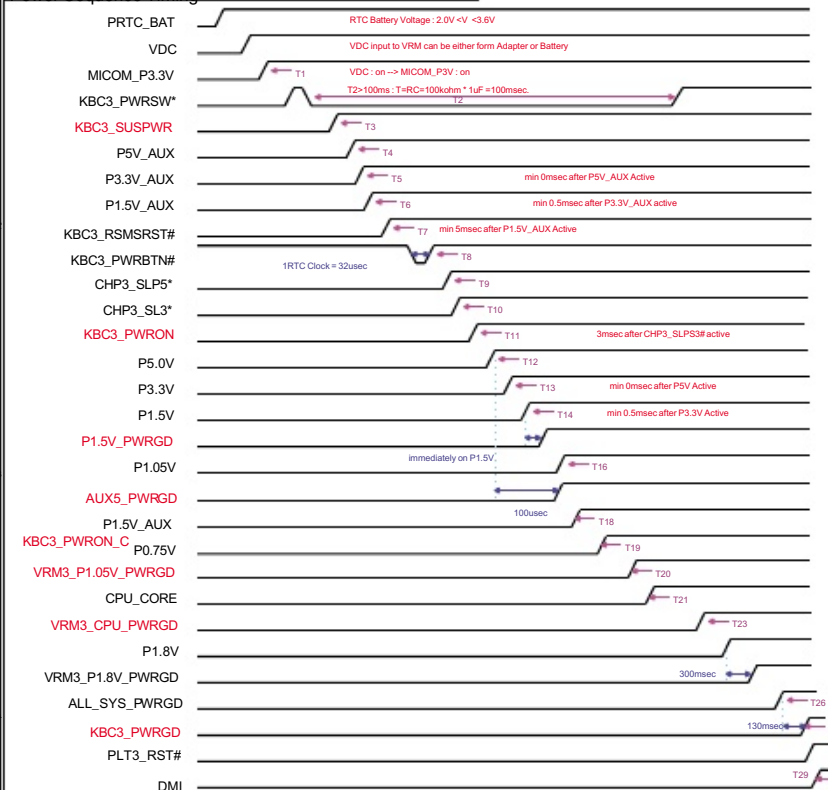
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Drawn	Qin wenchao	Rev	11/25/2011	11/2	Eric-VE-R	SAMSUNG
Check	Wu shijiang	Rev	PD		MAIN	ELECTRONICS
Approval	BC LEE	Rev	1.0		COVER	
Printed on		Printed on	December 13, 2011 16:40:00 PM	PAGE	1	OF 42

OPERATION BLOCK DIAGRAM



Power Sequence Timing



Devices	IDSEL#	REQ/INT#	Interrupts
USB	AD29(internal)	} Programmable	
Hub to PCI	AD30(internal)		
LPC Bridge/IDE/AC97/SMBUS	AD31(internal)		
Internal MAC	AD24(internal)		

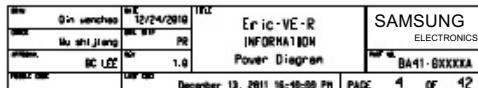
Devices	Address	Hex	Bus
TigerPoint	Master		SMBUS Master
CK-505M (Clock Generator)	1101001X	D2h	Clock, Unused Clock Output Disabled
SODIMM0	1010 000X	A0h	-
CPU Thermal Sensor	0111 100X	7Ah	Thermal Sensor

Port Number	ASSIGNED TO	Port Number	ASSIGNED TO
UHCL_0 0	USB Port_P0	UHCL_2 4	MMC
1	NC	5	Mini Card 2(For HSDPA)
UHCL_1 2	USB Port_P2	6	NC
3	Mini Card 1(For WLAN)	UHCL_3 7	CAMERA

PartNumber	ASSIGNED TO
1	Mini Card 1(Wireless LAN)
2	NC
3	LOM
4	NC

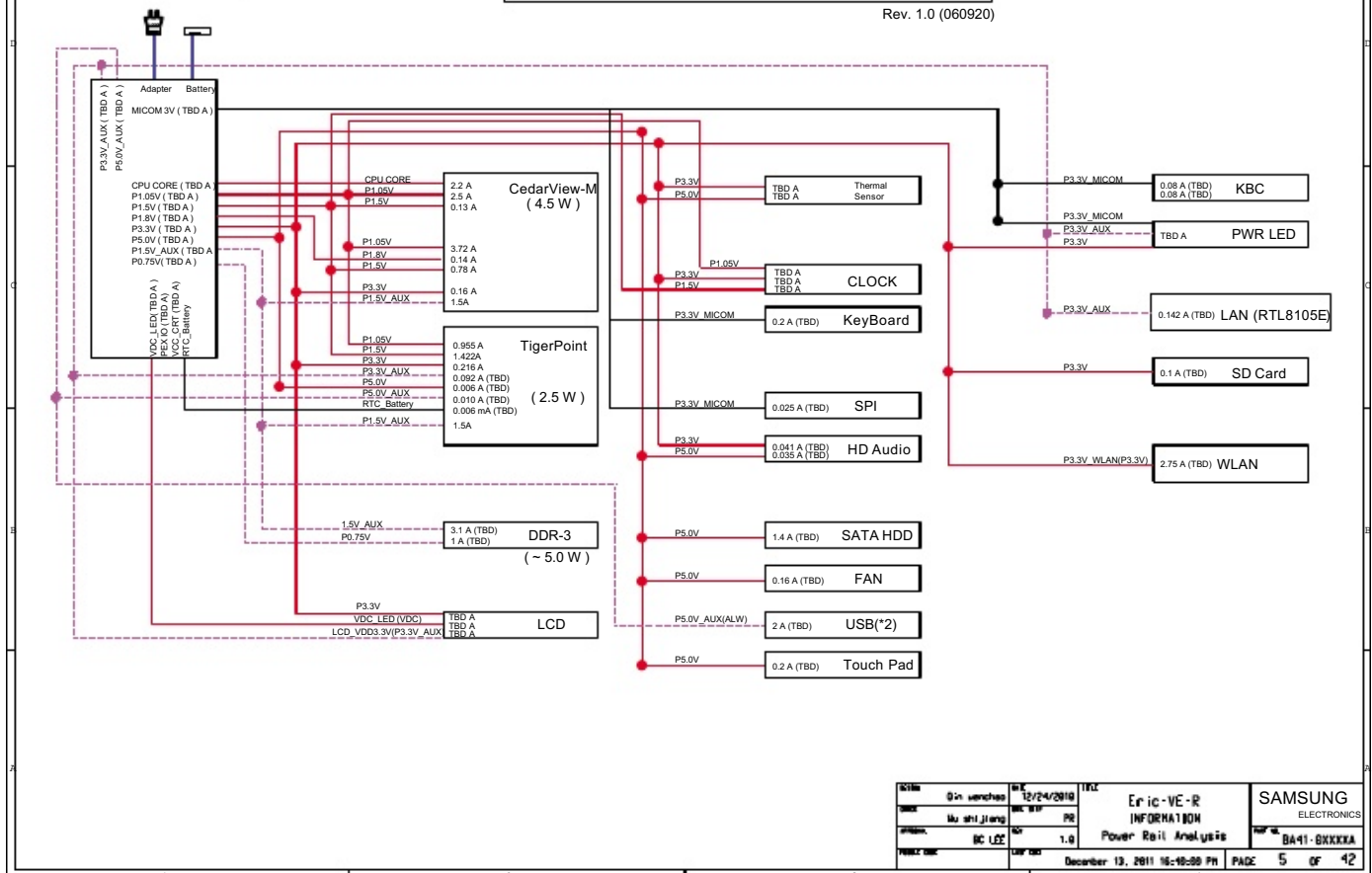
Power Rail	Descriptions
PRTC_BAT	3.3V (can drop to 2.0V min. in G3 state) supply for the RTC w/lev.
VDC	Primary DC system power supply (9 to 19V)
P1.05V(VCCP)	VTT for CPU, Calistoga & ICH1-M
P3.3V_MCOM	3.3V always power rail for MCOM
P1.5V	1.5V switched power rail (off in S3-S5)
P1.5V_AUX	1.5V power rail for DOR (off in S4-S5)
P0.75V	0.75V power rail for DOR (off in S4-S5)
PSV_AUX	5.0V power rail (off in S4-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
PSV	5.0V switched power rail (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
CPU_CORE	Core voltage for Atom CPU
GPU	Core voltage for Intel GPU

Site	Qin shenches	DATE	12/24/2010	Eric-VE-R	SAMSUNG ELECTRONICS
Book	Mu shi jiang	BOOK NO	PR	INFORMATION	
Empire	MC LEE	NO	1.0	Board Information	Part No BA41-0XXXXA
Project Book	UNP	DATE	December 13, 2011 16:10:00 PH	PAGE	3 OF 42



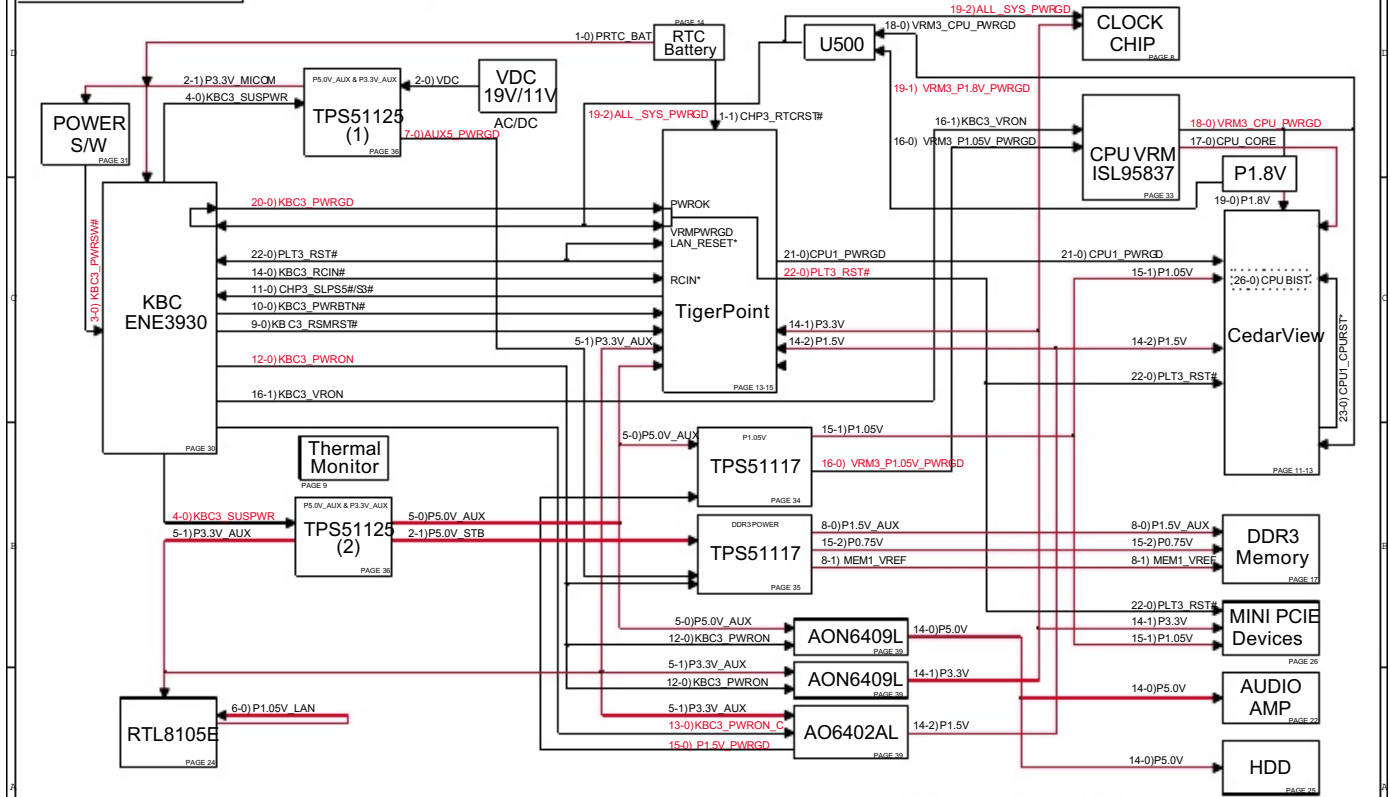
POWER RAILS ANALYSIS

Rev. 1.0 (060920)



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Desig	Wu shi jiang	Rev	PR	INFORMATION		ELECTRONICS
Proj	BC LCC	Ver	1.0	Power Rail Analysis	Part No	BA41-BXXXXA
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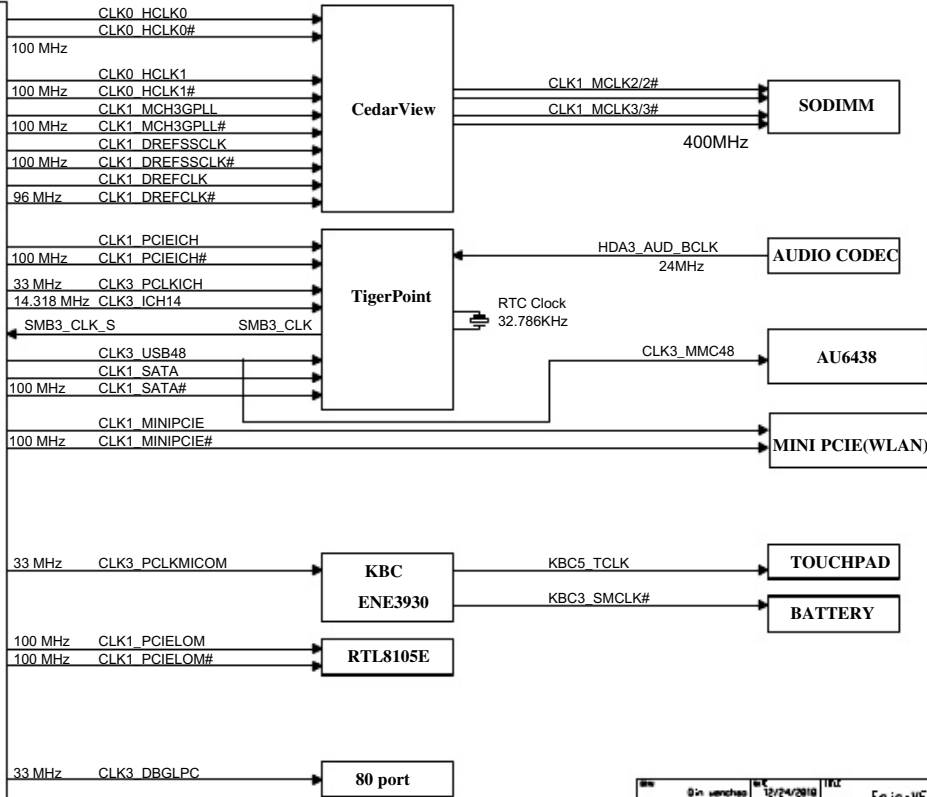
POWER SEQUENCE BLOCK DIAGRAM



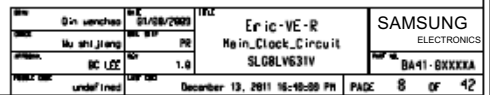
CLOCK DISTRIBUTION

CLOCK GENERATOR CK-505M SLG8LV631V

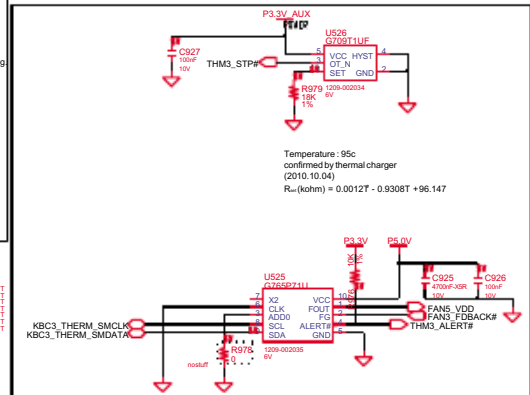
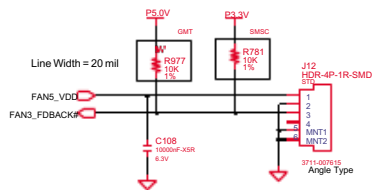
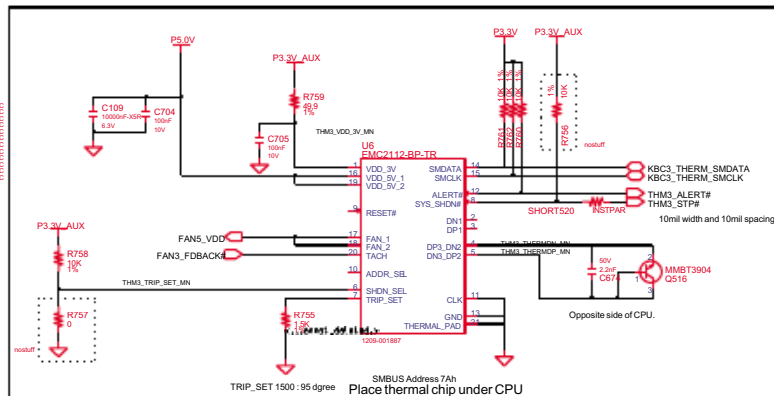
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Rev	0 in version	12/24/2010	Ver	1.0	Eric-VE-R	SAMSUNG
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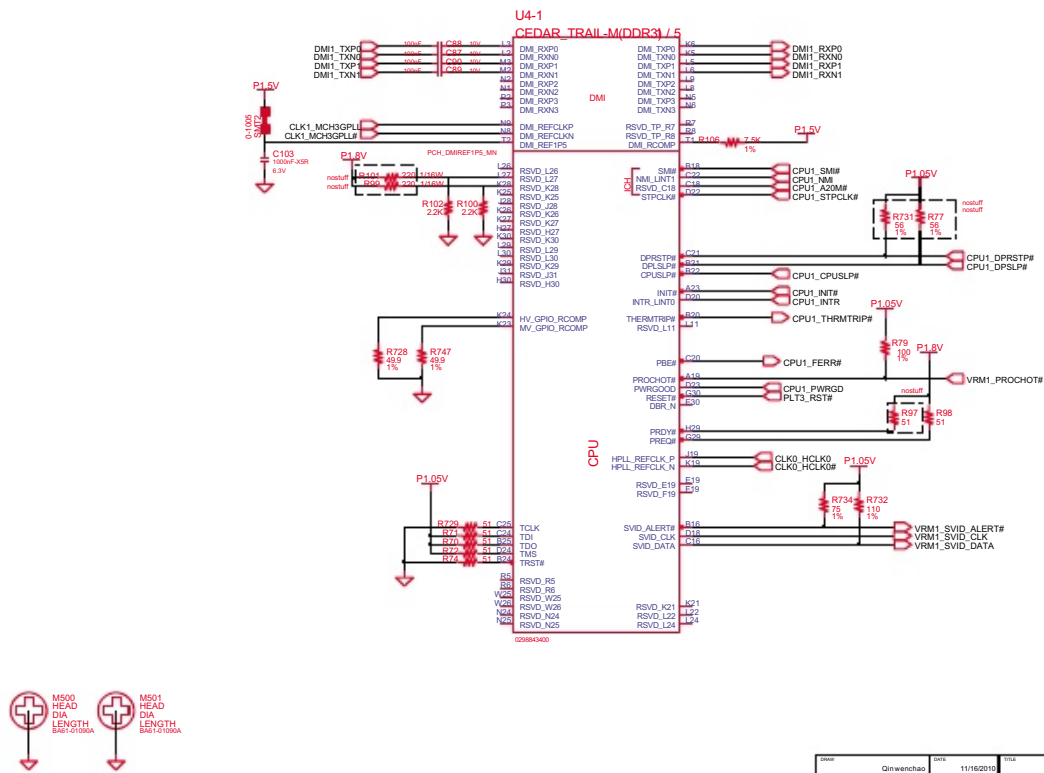


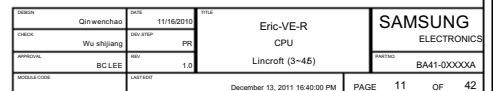
THERMAL SENSOR & FAN CONTROL



NAME	Qin wenchen	DATE	12/24/2019	TIME	
SN		MODEL	NR	Eric-VE-R	SAMSUNG
NAME	Wu shi jiang	MODEL	NR	Thermal Sensor ENC2112	ELECTRONICS
PHONE		SN	1.0	THERMAL SENSOR	BA91-6XXXXA
PHONE	BC 102	DATE			
PHONE		DATE	December 13, 2011 16:10:09 PH	PAGE	9 OF 42

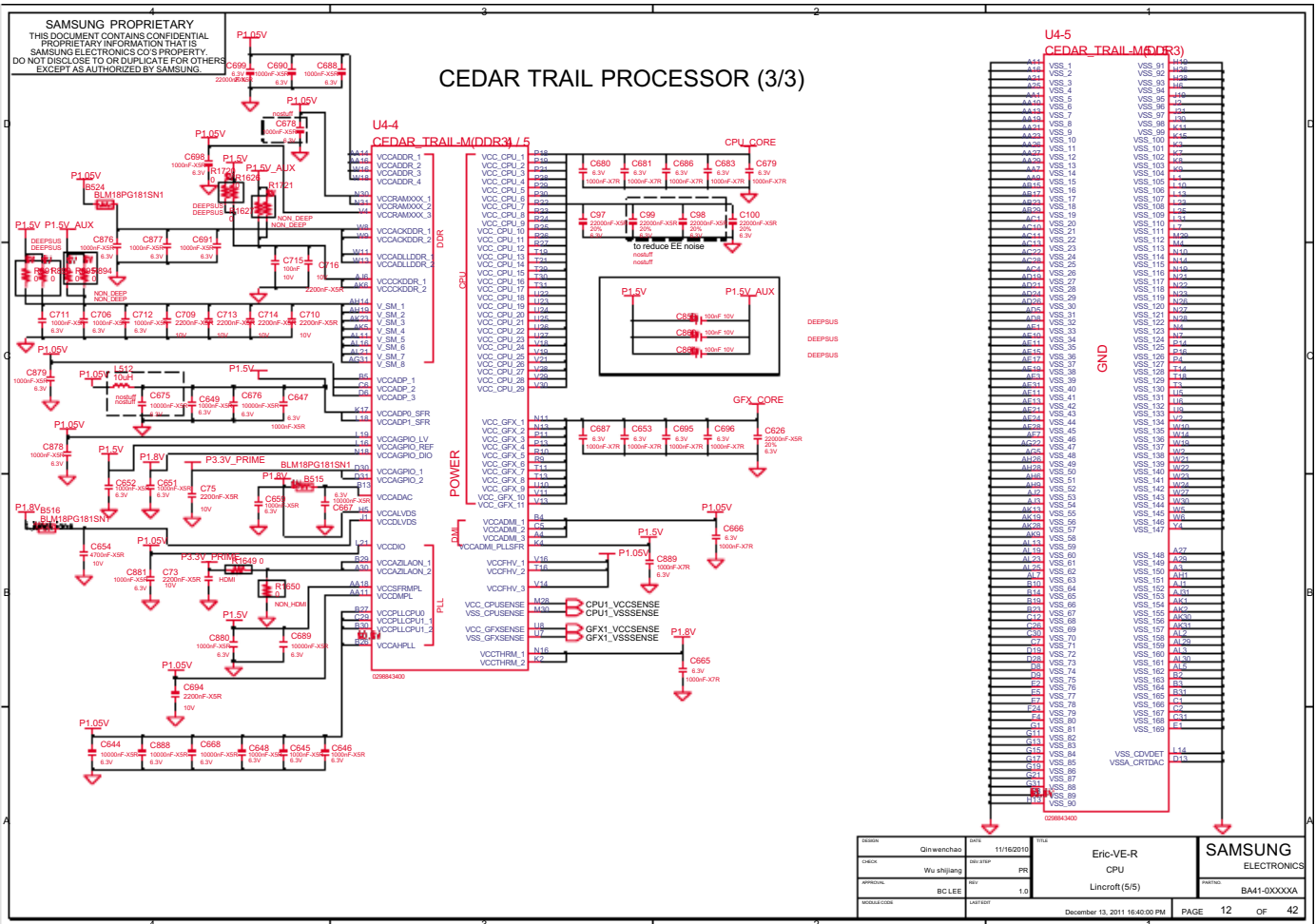
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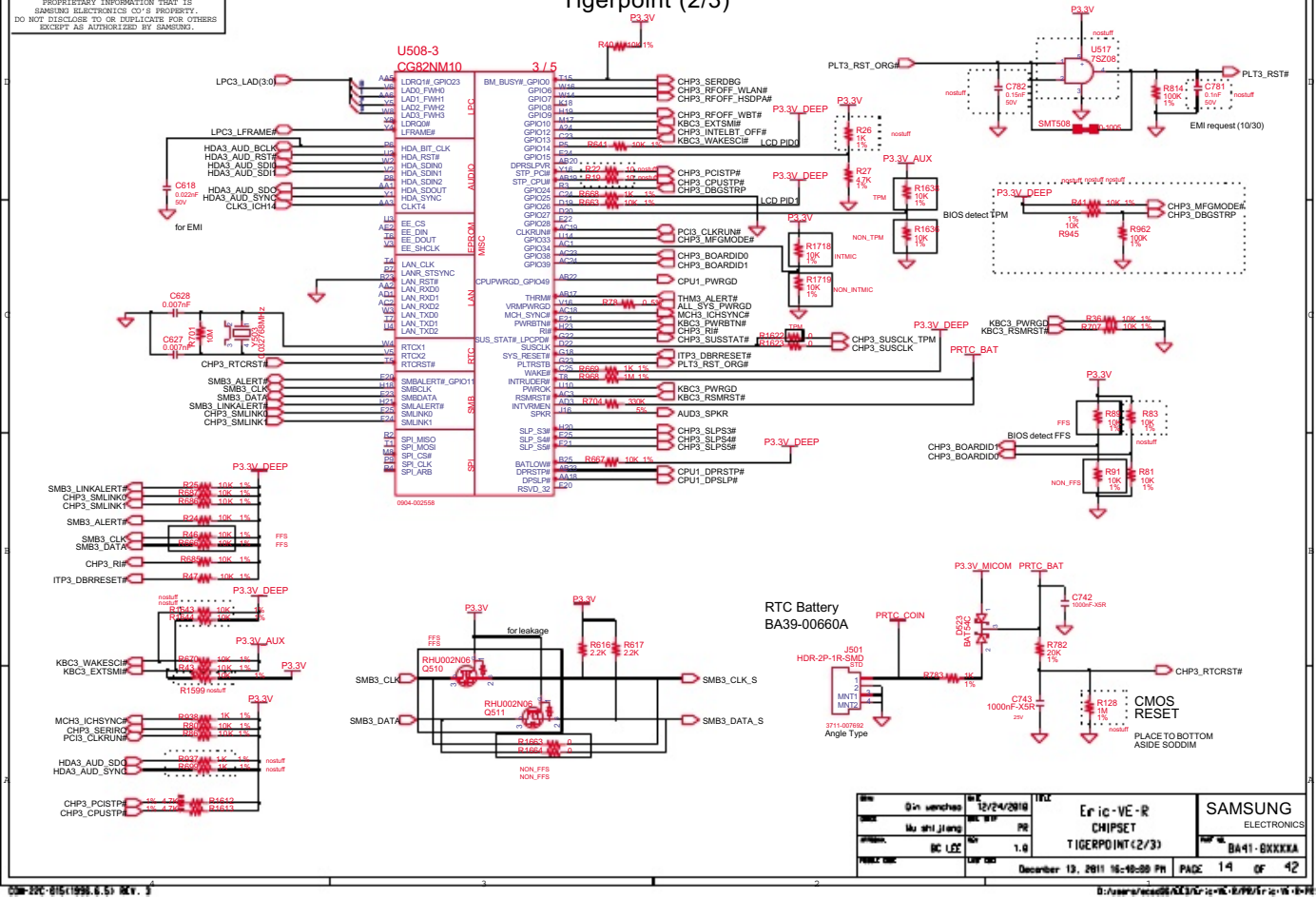
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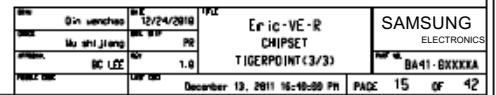
U4-5
CEDAR_TRAIL-M(DDR3)



DESIGNER	Qin-wenchao	DATE	11/16/2010	FILE	
CHECKER	Wu shijiang	REV	PR	Eric-VE-R	
APPROVAL	BC LEE	REV	1.0	Lincroft (5/5)	
WORKING CODE	14871001				

Tigerpoint (2/3)





80H DECODER CONNECTOR AND DEBUG CODE

ACPI/ASL Status Codes

01	System is entering S1 sleep state
02	System is entering S2 sleep state
03	System is entering S3 sleep state
04	System is entering S4 sleep state
05	System is entering S5 sleep state
10	System is waking up from the S1 sleep state
20	System is waking up from the S2 sleep state
30	System is waking up from the S3 sleep state
40	System is waking up from the S4 sleep state
50	System is waking up from the S5 sleep state
AA	System has transitioned into ACPI mode (ACPI)

PEI Status Codes

```

10 Process Codes
11 01 PEI Core is started
12 Pre-memory CPU initialization (CPU module specific)
13 Pre-memory CPU initialization (CPU module specific)
14 Pre-memory CPU initialization (CPU module specific)
15 Pre-memory North Bridge initialization (North Bridge module specific)
16 Pre-memory North Bridge initialization (North Bridge module specific)
17 Pre-memory North Bridge initialization (North Bridge module specific)
18 Pre-memory South Bridge initialization (South Bridge module specific)
19 Pre-memory South Bridge initialization (South Bridge module specific)
20 Pre-memory South Bridge initialization (South Bridge module specific)
21 2A OEM Pre-memory initialization (OEM module specific)
22 2B OEM Pre-memory initialization (OEM module specific)
23 2C OEM Pre-memory initialization (OEM module specific)
24 Memory initialization, Programming memory timing information
25 Memory initialization (other)
26 Memory initialization (other)
27 Memory initialization (other)
28 Memory Installed
29 CPU post-memory initialization is started
30 CPU post-memory initialization is started
31 CPU post-memory initialization is started
32 CPU post-memory initialization, Boot Strap Processor (BSP) selection
33 CPU post-memory initialization, Boot Strap Processor (BSP) selection
34 CPU post-memory initialization, Boot Strap Processor (BSP) selection
35 Pre-Memory North Bridge initialization is started
36 Pre-Memory North Bridge initialization (North Bridge module specific)
37 Pre-Memory North Bridge initialization (North Bridge module specific)
38 Pre-Memory North Bridge initialization (North Bridge module specific)
39 Pre-Memory South Bridge initialization (South Bridge module specific)
40 Pre-Memory South Bridge initialization (South Bridge module specific)
41 Pre-Memory South Bridge initialization (South Bridge module specific)
42 Pre-Memory South Bridge initialization (South Bridge module specific)

```

PEI Error Codes

```

0x00000000 Memory initialization error Invalid memory type or incompatible memory speed.
0x00000001 Memory initialization error Invalid memory size or memory modules do not match
0x00000002 Memory initialization error Invalid memory detected
0x00000003 Unspecified memory initialization error
0x00000004 Memory not installed
0x00000005 Invalid CPU type/speed
0x00000006 CPU mismatch
0x00000007 CPU self test failed or possible CPU cache error
0x00000008 Micro-code not found or micro-code update is failed
0x00000009 Internal CPU error
0x0000000A reset PR is not available
0x0000000B Reserved for future AMI error codes

```

Recovery Progress Codes

F0	Recovery condition triggered by firmware(Auto recovery)
F1	Recovery condition triggered by user(Forced recovery)
F2	Recovery process started
F3	Recovery firmware image is found
F4	Recovery firmware image is loaded
F5-F7	Reserved for future AMI progress codes

Recovery Error Codes

Recovery Error Codes

- F8 Recovery PRI is not available
- F9 Recovery capsule is not found
- FA Invalid recovery capsule
- FB-FF Reserved for future AMI error codes
- 5A Internal CPU error
- 5B reset PRI is not available
- 5C-5E Reserved for future AMI error codes

DXE Status Codes

Progress Codes

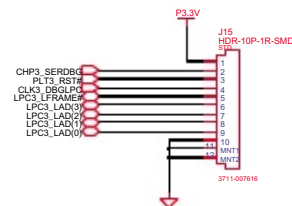
```

60 DEX Core & started
61 Installation & the South Bridge Runtime Services
62 CPU DEX initialization is started
63 CPU DEX initialization (CPU module specific)
64 CPU DEX initialization (CPU module specific)
65 CPU DEX initialization (CPU module specific)
66 CPU DEX initialization (CPU module specific)
67 CPU DEX initialization (CPU module specific)
68 CPU DEX initialization (CPU module specific)
69 North Bridge DEX initialization is started
70 North Bridge DEX initialization (North Bridge module specific)
71 North Bridge DEX initialization (North Bridge module specific)
72 North Bridge DEX initialization (North Bridge module specific)
73 North Bridge DEX initialization (North Bridge module specific)
74 North Bridge DEX initialization (North Bridge module specific)
75 North Bridge DEX initialization (North Bridge module specific)
76 South Bridge DEX initialization is started
77 South Bridge DEX initialization (South Bridge module specific)
78 South Bridge DEX initialization (South Bridge module specific)
79 South Bridge DEX initialization (South Bridge module specific)
80 South Bridge DEX initialization (South Bridge module specific)
81 South Bridge DEX initialization (South Bridge module specific)
82 South Bridge DEX initialization (South Bridge module specific)
83 M initialization
84 Reserved for future AMI DEX codes
85 OEM DEX initialization codes
86 BIOS Event Service (BIOS Event codes are started)
87 Driver controller is started
88 Bus initialization is started
89 Bus Iot/Plug Controller Initialization
90 Bus Enumeration
91 Bus Request Resources
92 Bus Assign Resources
93 Console CUI devices connect
94 Console I/O devices connect
95 Use initialization is started
96 Use Reset
97 Use Detect
98 Use Enable
99 Reserved for future AMI codes
A0 DEX initialization is started
A1 DEX Reset
A2 DEX Enable
A3 DEX Disable
A4 SCSI Initialization is started
A5 SCSI Detect
A6 SCSI Enable
A7 Setup Verifying Password
A8
A9
AA
AB
AC Reserved for future AMI codes (see ASL Status Codes section below)
AD
AE Reserved for ASL (see ASL Status Codes section below)
AF Ready to Boot event
B0 Legacy Boot Event
B1 Exit Boot Services event
B2 Runtime Set Virtual Address MAP Begin
B3 Runtime Set Virtual Map End
B4 Legacy Console ROM Initialization
B5
B6
B7
B8
B9
BA
BB
BC
BD
BE
BF Reserved for future AMI codes
C0 BIOS Reset

```

DXE Error Codes

D0	CPU initialization error
D1	North Bridge initialization error
D2	South Bridge initialization error
D3	Some of the Architectural Protocols are not available
D4	PCI resource allocation error.Out of Resources
D5	No Space for Legacy Option ROM
D6	No Console Output Devices are found
D7	No Console Input Devices are found
D8	Invalid password
D9	Error loading Boot Option(Loadimage returned error)
DA	Boot Option is failed(Startimage returned error)
DB	Flash update is failed
DC	Reset protocol is not available



DATE	Qin wenchao	DATE	12/24/2018	TYPE	Eric-VE-R	SAMSUNG	
NAME	Ma shi jiang	NAME	PR		SPLB10S_ROM	ELECTRONICS	
VERSION	BC 1.0	VER	1.0		SPLB10S_ROM	REF ID:	BA41-BXXXXA
PUBLIC TIME		UPD TIME		December 13, 2011 16:40:50 PM	PAGE	16	OF 42



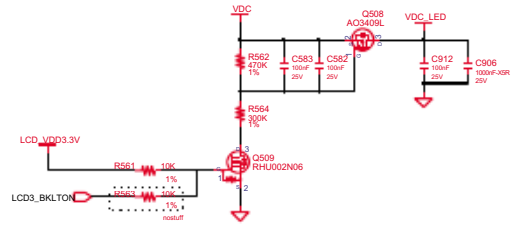
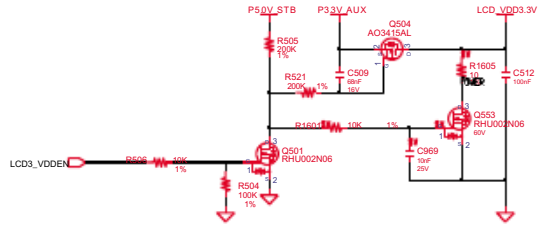
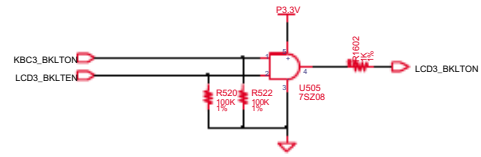
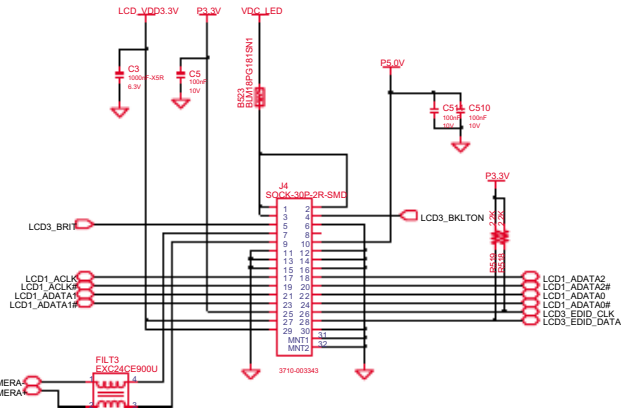


ERIC-VE-R
GRAPHICS [F
ORI

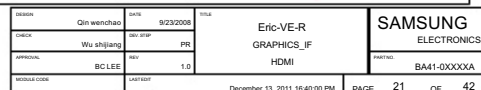


SAMSUNG PROPRIETARY

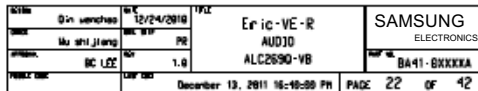
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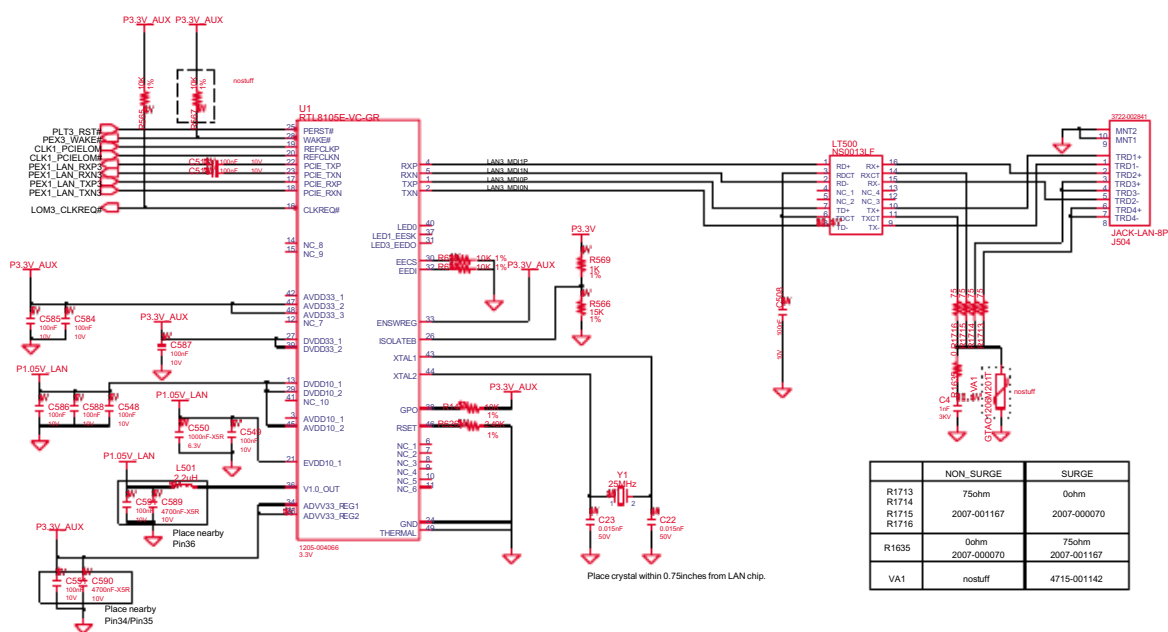
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DATE	12/24/2018	REV	1.0	DESIGNER	Eric-VE-R	GRAPHICS_I/F
DATE	12/24/2018	REV	1.0	DESIGNER	Eric-VE-R	LED_LCD_I/F
DATE	12/24/2018	REV	1.0	DESIGNER	Eric-VE-R	BA41-BXXXXA
DATE	12/24/2018	REV	1.0	DESIGNER	Eric-VE-R	BA41-BXXXXA
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DATE	12/24/2018	REV	1.0	DESIGNER	Eric-VE-R	BA41-BXXXXA
DATE	12/24/2018	REV	1.0	DESIGNER	Eric-VE-R	BA41-BXXXXA
DATE	12/24/2018	REV	1.0	DESIGNER	Eric-VE-R	BA41-BXXXXA



Audio Codec should be soldered by ALC269Q-VB2-GR that is new.



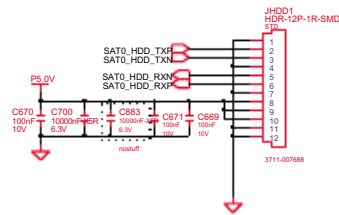
Realtek RTL8105E



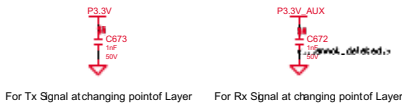
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R1713	75ohm	0ohm
R1714		
R1715	2007-001167	2007-000070
R1716		
R1635	0ohm	75ohm
	2007-000070	2007-001167
VA1	nostuff	4715-001142

SATA I/F CONN

SATA HDD CONN



For EMI



DATE	01/11/2011	REV	12/24/2010	FILE	Eric-VE-R	SAMSUNG
DESIGNER	Yu shi Jiang	PE			SATA_DEVICES	ELECTRONICS
DESIGN	BC LCC	REV	1.0		SATA I/F	BA91-0XXXXA
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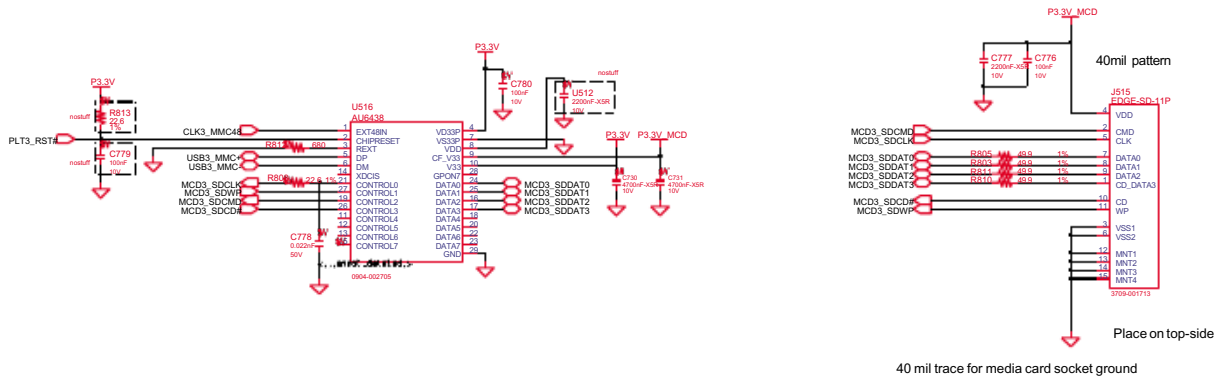


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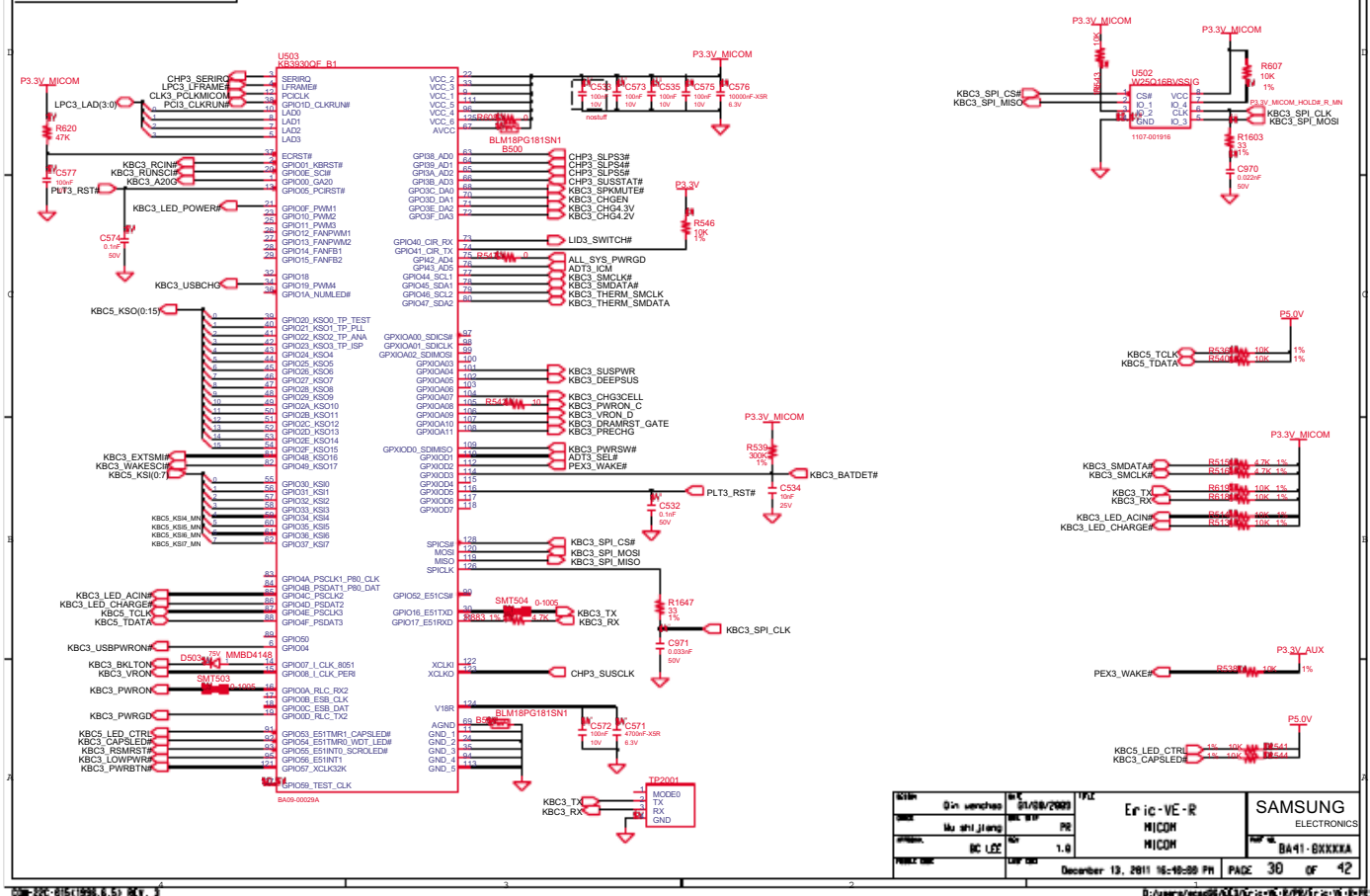
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MMC(AU6438)

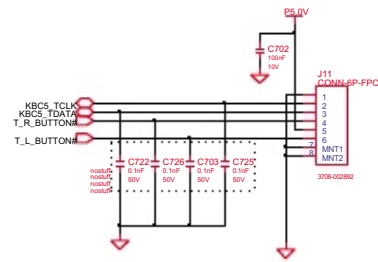


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Rev	01	Des	Eric-VC-R	DATE	12/24/2010	FILE	Eric-VC-R
Drawn	Eric-VC-R	Check	Eric-VC-R	DATE	12/24/2010	FILE	Eric-VC-R
Rev	01	Des	Eric-VC-R	DATE	12/24/2010	FILE	Eric-VC-R
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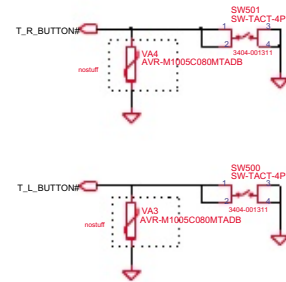
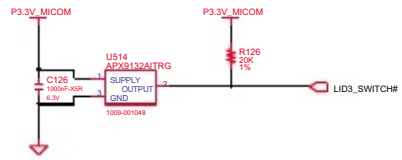
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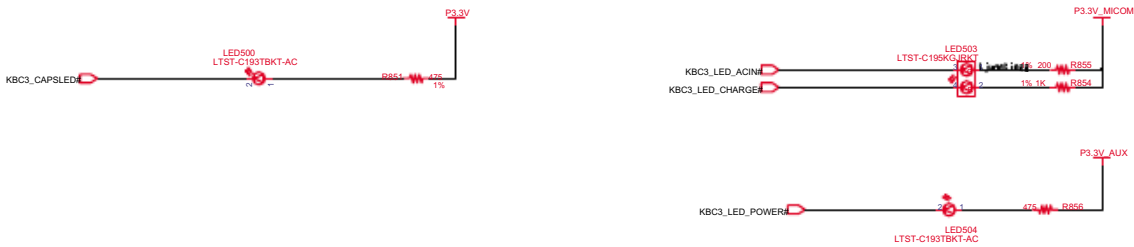
TOUCHPAD



LID SWITCH

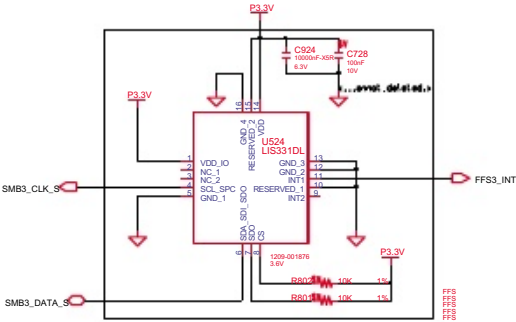
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LED SWITCH LOGIC



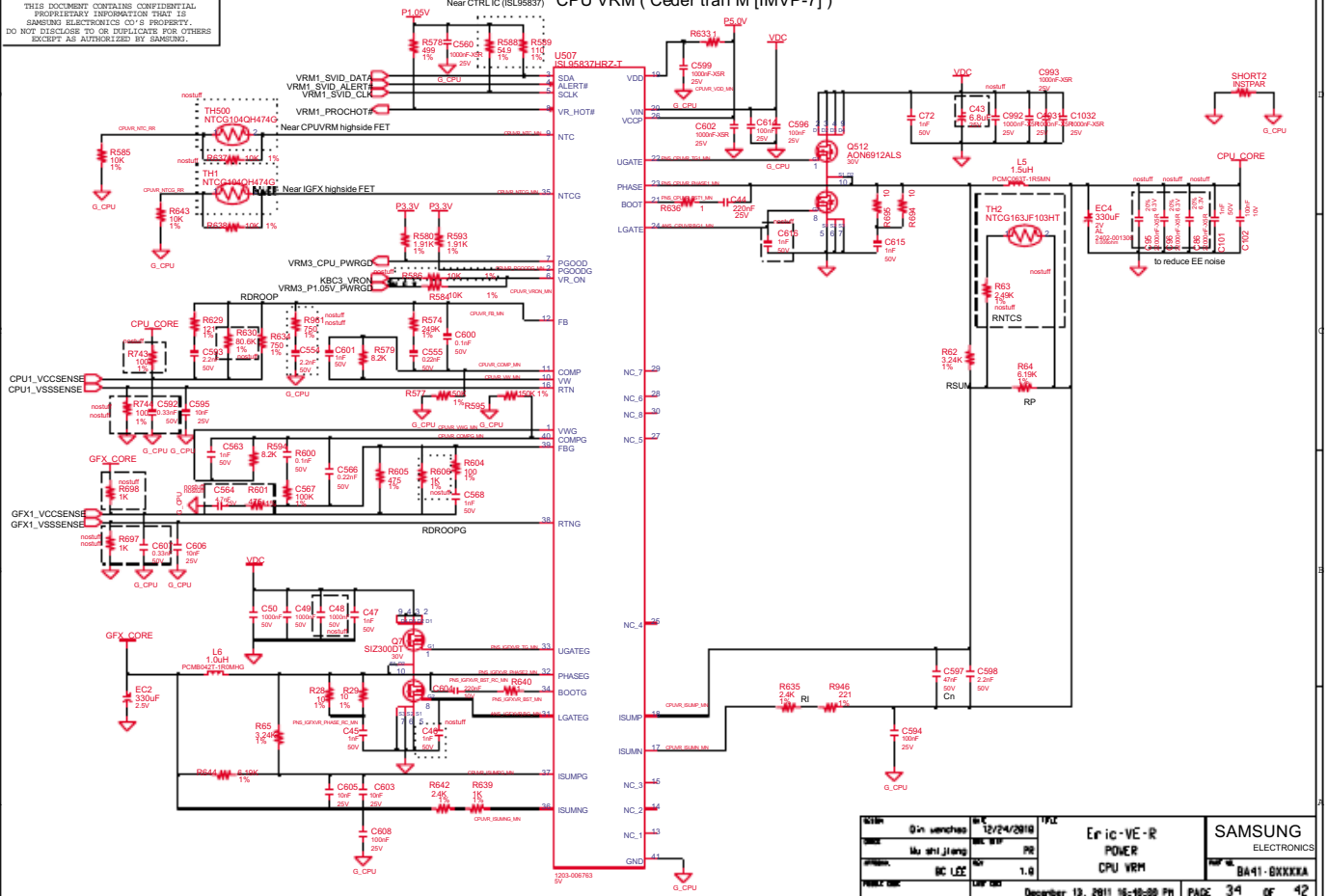
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Print Date	December 13, 2011 16:48:59 PM	PAGE	32	OF	42

FREE FALL SENSOR

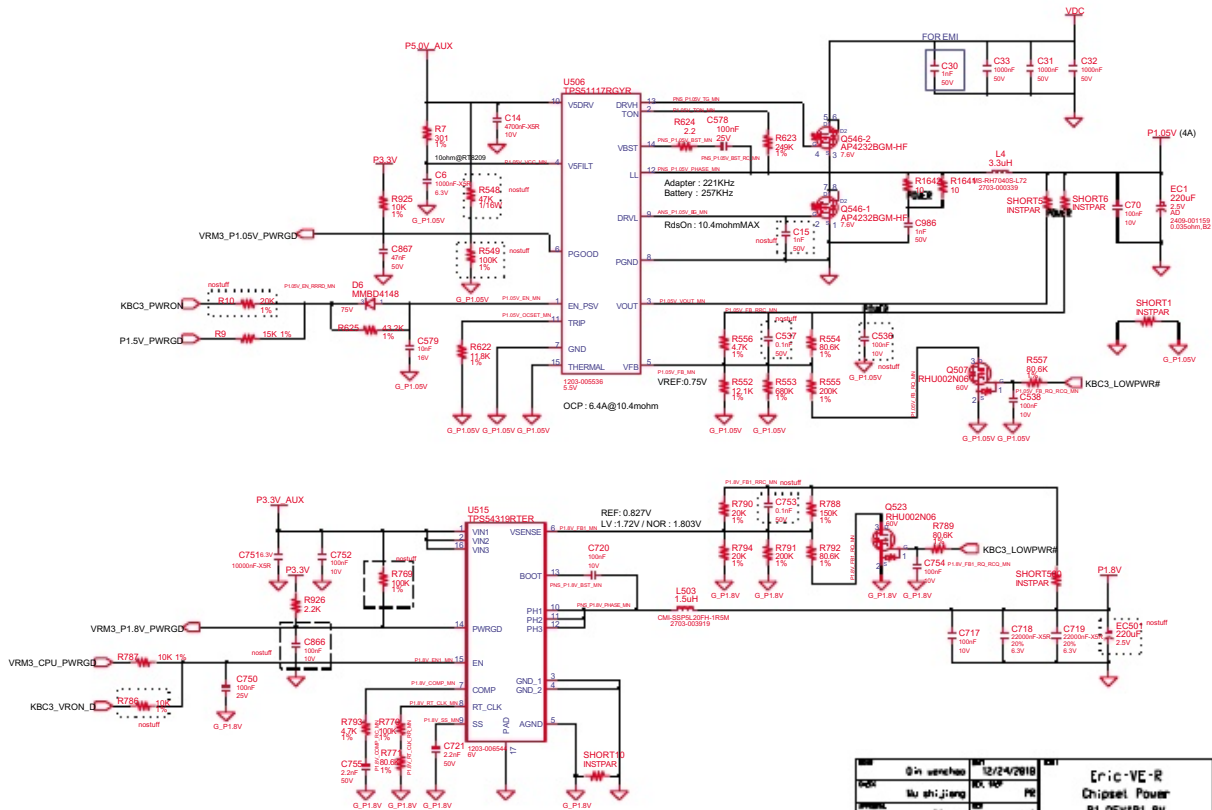


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Des	Mu shi Jiang	PE	FFS	ELECTRONICS
Proj	BC LCC	1.0	FreeFallSensor	BA41-0XXXXA
Print Date	undefined	December 13, 2011 16:40:09 PM	PAGE 33	OF 42

CPU VRM (Ceder trail M [IMVP-7])



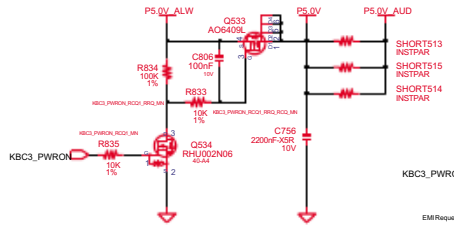
Chipset Power (P1.8V & P1.05V)



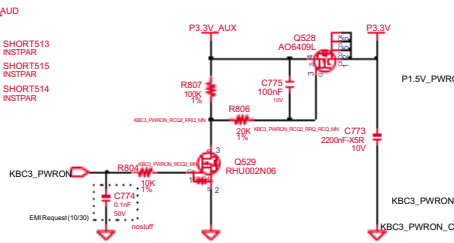
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Wu shijiang	12/24/2018	Chipset Power	ELECTRONICS
BC LEE	1.0	P1.05V&P1.8V	BA91-8XXXX
Under: rmd	December 13, 2011 16:40:00 PM	PAGE 35	OF 42



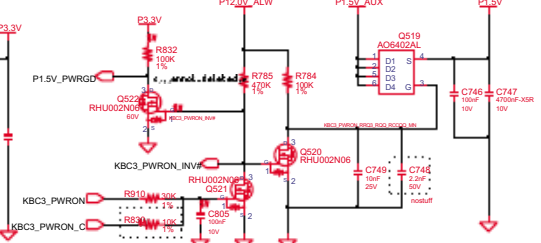
Load Switch Control (P5.0V)



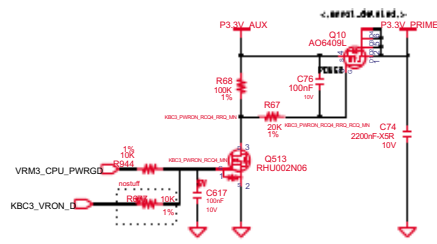
Load Switch Control (P3.3V)



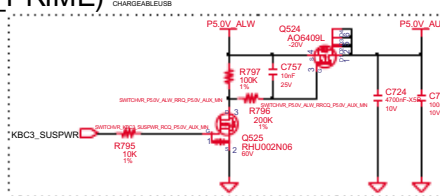
Load Switch Control (P1.5V)



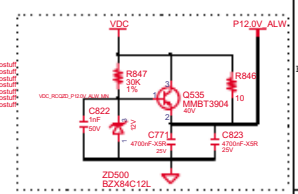
Load Switch Control (P3.3V_PRIME)



Sleep'n Charger



P12V_ALW



For Non-CHARGEABLE USB

Rev	0 in version	12/24/2018	19L	Eric-VC-R	SAMSUNG
Auth	Mu shi Jiang	PE		Switched PWR	ELECTRONICS
PrjNm	BC LCC	1.0		Switched PWR	BA91-0XXXXA
Rev					
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